Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Original) A method of forming a PFET device comprising the steps:

providing a substrate having at least one gate stack;

depositing a silicon nitride layer by means of a dual-frequency plasma enhanced CVD process, the CVD process comprising a temperature in the range 400 °C to 550 °C;

forming a spacer on said at least one gate stack from said silicon nitride layer; and

forming a PFET device comprising said at least one gate stack having said spacer.

2. (Original) The method of claim 1 wherein said dual-frequency plasma enhanced CVD process further comprises a pressure in the range 2 Torr to 5 Torr.

3. (Original) The method of claim 1 wherein said dual-frequency plasma enhanced CVD process further comprises a low frequency power in the range 0 W to 50 W.

4. (Original) The method of claim 1 wherein said dual-frequency plasma enhanced CVD process further comprises a high frequency power in the range 90 W to 110 W.

5. (Original) The method of claim 1 wherein said dual-frequency plasma enhanced CVD process further comprises precursor gases of silane, ammonia and nitrogen at flow rates in the ratio 240:3200:4000 sccm.

6. (Original) The method of claim 1 wherein said dual-frequency plasma enhanced CVD process further comprises a temperature of 480 °C.

7. (Original) The method of claim 1 wherein said dual-frequency plasma enhanced CVD process further comprises a pressure of 2.5 Torr.

8. (Original) The method of claim 1 wherein said dual-frequency plasma enhanced CVD process further comprises a high frequency power of about 100 W and a low frequency power of about 40 W.

9. (Original) A method of forming a PFET device comprising the steps:

providing a substrate having at least one gate stack;

depositing a silicon nitride layer by means of a dual-frequency plasma enhanced CVD process, the CVD process comprising a temperature in the range 400 °C to 550 °C, a pressure in the range 2 Torr to 5 Torr, a low frequency power in the range 0 W to 50 W, a high frequency power in the range 90 W to 110 W, and precursor gases of silane, ammonia and nitrogen at flow rates in the ratio about 240:3200:4000 sccm;

forming a spacer on said at least one gate stack from said silicon nitride layer; and

forming a PFET device comprising said at least one gate stack having said spacer.

10. (Original) The method of claim 9 wherein the CVD process comprises a temperature about 480 °C, a pressure of about 2.5 Torr, a low frequency power of about 40 W, a high frequency power of about 100 W, and precursor gases of silane, ammonia and nitrogen at flow rates in the ratio about 240:3200:4000 sccm.

11. (Withdrawn - currently amended) A silicon nitride film for forming a semiconductor device having a spacer, said spacer comprising a silicon nitride film formed by a dual-frequency PECVD process comprising a temperature in the range 400 °C to 550 °C, wherein said silicon nitride film has a vertical to horizontal coverage ratio between 70 % to 90%.

12. (Withdrawn) The silicon nitride film of claim 11 further comprising RBS Si, N, H ratios of 0.4:0.48:0.12.

13. (Withdrawn) The silicon nitride film of claim 11 further comprising a FTIR ratio of Si-H/N-H of about 0.1.

14. (Withdrawn) The silicon nitride film of claim 11 further comprising percent bonded hydrogen less than 10% by volume.

15. (Withdrawn) The silicon nitride film of claim 11 further comprising a refractive index of 1.95 ± 0.05.

16. (Withdrawn) The silicon nitride film of claim 11 wherein said silicon nitride film has a deposited stress in the range from about + 8 Gigadynes/cm2 tensile stress to -7 Gigadynes/cm2 compressive stress.

17. (Withdrawn) The silicon nitride film of claim 11 wherein said silicon nitride film has a deposited stress of about 3 Gigadynes/cm2 compressive stress.

18. (Withdrawn) A semiconductor device having a spacer, wherein said spacer comprises a silicon nitride film formed by a dual-frequency PECVD process comprising a temperature in the range 400 °C to 550 °C, wherein said silicon nitride film has a vertical to horizontal coverage ratio between 70 % to 90%.

19. (Withdrawn) The semiconductor device of claim 18 wherein said semiconductor device is a PFET device.

20. (Withdrawn) The semiconductor device of claim 19 where in said spacer comprises a dual spacer.